



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,021	08/14/2001	Monte Mar	CYPR-CD00174	1938

7590 04/26/2004

WAGNER, MURABITO & HAO LLP  
Third Floor  
Two North Market Street  
San Jose, CA 95113

EXAMINER

PERVEEN, REHANA

ART UNIT	PAPER NUMBER
----------	--------------

2116

DATE MAILED: 04/26/2004

7

Please find below and/or attached an Office communication concerning this application or proceeding.

226

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	09/930,021		MAR ET AL	
	<b>Examiner</b>		<b>Art Unit</b>	
	Rehana Perveen		2116	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 February 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>6</u> .   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Myers et al, Patent No. 6,185,127.

As to claims 1 and 10, Myers et al teach receiving configuration information into a configuration register (figure 1, one of configuration registers 12-15) of a multi-function device (figure 1, device 10), the device comprising a plurality of analog blocks coupled in a single integrated circuit (abstract), the plurality of analog functional blocks comprising a first set of analog blocks that can be selectively and electrically coupled to and decoupled from another analog block, the configuration information is for selectively and electrically coupling analog blocks in a particular configuration according to an analog function to be performed, and coupling electrically selected analog blocks according to the configuration information in the configuration register to achieve the analog function (figure 1, col. 2 line 45 – col. 3 line 37).

As to claims 2 and 11, Myers et al teach changing dynamically the configuration information to achieve a different analog function (col. 11 lines 50-67).

As to claims 3 and 12, Myers et al teach the configuration information in the configuration register is for specifying inputs and outputs of each of the analog blocks according to the analog function (abstract and col. 3 lines 15-37).

As to claims 4 and 13, Myers et al teach an analog block comprises a plurality of analog elements having changeable characteristics wherein the configuration register is for specifying characteristics of the analog elements according to the analog function (col. 1 lines 39-67).

As to claims 5, 6, 16, and 17, Myers et al teach the receiving of configuration information is performed during bootup (inherent for a normal configuration process to receive the configuration information during bootup) or during program execution subsequent to bootup of a system comprising the device (inherent for changing the analog function after bootup to change the characteristics).

As to claims 7, 8, 14, 15, and 29, Myers et al teach the analog blocks comprises switched capacitor blocks or continuous time blocks (inherent in prior art systems).

As to claims 9 and 18, Myers et al teach storing an address for the configuration register in a register bank (figure 1, col. 4 lines 11-53).

As to claim 19, Myers et al inherently teach setting a bit in the configuration register to a first value to include a compensating capacitor when the analog block is to perform a comparator function (inherent for comparator function selection, col. 7 lines 1-15) and to a second value to bypass the compensating capacitor (inherent for comparator function disablement, col. 7 lines 1-15).

As to claim 20, Myers et al teach setting bits in the configuration register to specify a power level for the analog block (col. 4 lines 20-66).

As to claims 21 and 22, Myers et al teach setting bits in the configuration register to specify a resistance of a resistor or to specify a capacitance of a capacitor in the analog block (col. 1 lines 65-67).

As to claims 23 and 24, Myers et al teach setting a bit in the configuration register to change the phase of an input or to select a clock phase for sampling an input to the analog block (col. 5 lines 6-14 and col. 7 lines 1-15).

As to claim 25, Myers et al inherently teach setting a bit in the configuration register to control a gated switch in the analog block (inherent, col. 7 lines 1-15).

Art Unit: 2116

Claims 26-29 are directed to various combinations of limitations already claimed in claims 1-25. Myers et al teach all of the limitations as stated above in claims 1-25. Therefore, Myers et al also teach the claims 26-29.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rehana Perveen whose telephone number is 703-305-8476. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Rehana Perveen  
Primary Patent Examiner  
Technology Center 2100